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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/541,773	04/03/2000	Bryan Keith Bullis	RAL9-99-0137	4749

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IBM CORPORATION
PO BOX 12195
DEPT 9CCA, BLDG 002
RESEARCH TRIANGLE PARK, NC 27709

EXAMINER
LEE, TIMOTHY L

ART UNIT	PAPER NUMBER
2697	5

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/541,773	BULLIS ET AL.	
	Examiner	Art Unit	
	Timothy Lee	2697	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11* is/are allowed.

6)☒ Claim(s) *1-6,8,9 and 12-19* is/are rejected.

7)☒ Claim(s) *7,10 and 20-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5 and 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Egbert et al. (US 6,115,387).

3. Regarding claims 1 and 12, Egbert et al. discloses a method for initiating and forwarding data from a device as a function of the data received at the device. Fig. 1 shows the entire device that acts as a switching element. Fig. 3 is a more detailed view of the internal workings of the switch. The switch includes an external memory interface 34 that connects to the external SDRAM 36, which is shown in Fig. 1. The switch has three modes of operation. The switch mode that applies to the input (i.e. receive) port determines forwarding latency, or how soon the switch 12 will forward a frame once it begins receiving the frame. In all three of the modes, frame data received at the receive FIFO 52 of an internal MAC (see Fig. 1) port is forwarded to a buffer 140 in the external memory 36 as soon as possible. See col. 20, lines 48-65. In other words, the switch receives data through the various ports on the switch and immediately transfers the data to an external RAM that acts as a holding area for the data before it is switched to its next destination. Looking at it in this way, the entire switching system can be considered a data buffer (a data buffer for buffering a data cell). In switching the data that is being held in the

external memory 36, the data is first transferred to output queues 74, where it is determined what kind of latency will be applied to the data—the output queues 74, as shown in Fig. 3, can be considered an entry section (comprising an entry section). The transmission of data is controlled by the buffer manager 72, which begins moving frame data from the address specified by the frame pointer, and once the transmit FIFO of the MAC port has been primed to its start point, frame transmission commences—thus, the buffer manager 72 when data should be transmitted from one section to another (a signaling circuit coupled to the entry section for providing a signal to transfer a portion of data). In the first mode of the switch operation designed to provide the lowest latency, frames are received and forwarded at line-rate speed. In this mode, frame reception may not complete before frame transmission at the output ports commences (transfer a portion of a data cell prior to the data cell being completely received by the entry section). See col. 20, line 56-col. 21, line 36.

4. Regarding claim 2, Egbert et al. discloses that the port vector FIFO that there can be different thresholds, including receiving n bytes where n <64 bytes (signal is provided once the amount of data received by the entry section reaches a predetermined threshold). See col. 22, lines 1-11.

5. Regarding claim 3, the output queues 74 could be considered entry sections along with being buffer entry sections.

6. Regarding claim 4, Egbert et al. discloses that the system was designed as a switch for a packet switched network. As an example, ATM is a packet switched system. ATM is asynchronous (wherein signaling circuit comprises an asynchronous signaling circuit).

7. Regarding claim 13, the buffer manager controls all transmission of data across the switch, so by issuing a command for the output queue to receive data from the external memory, the output queue could begin receiving a new data cell before it is finished output the previous cell depending on when that command is issued.

8. Regarding claim 14, the output queues contain a read side and a write side as shown in Fig. 3 (buffer entry section comprises a write element and a read element). Egbert et al. also discloses that the system was designed as a switch for a packet switched network. As an example, ATM is a packet switched system. ATM is asynchronous (wherein signaling circuit comprises an asynchronous signaling circuit).

9. Regarding claim 15, the buffer controller controls all of the movement of data through the switch, so it is responsible for telling the output queues when to forward their data and for telling when the output queue should receive its data from the external memory (add signaling portion and a remove signaling portion).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 5, 6, 8, 9, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egbert et al.. The limitations of claims 4 and 12 have been addressed above.

12. Regarding claims 5, Egbert et al. discloses that the output queues contain a read side and a write side as shown in Fig. 3 (buffer entry section comprises a write element and a read element). Queuing takes the form of the port vector FIFO 70 writing frame pointers into the various output queues 74 indicated in a forwarding port vector—these pointers must be responsible for keeping track where in the data it is being transmitted (entry pointer...an item pointer). See col. 10, lines 1-11. Egbert et al. does not expressly disclose having an entry counter within the buffer entry section, but Egbert et al. does disclose having an MIB counter region that keep tracks of statistics of all the ports. See col. 11, lines 36-42. It would have been obvious to put this counter functionality into the output queues section. One would have been motivated to do this because having the counters on the chip would allow for faster access to the values contained in the counters.

13. Regarding claim 8, the claim includes the same limitations recited in claims 1-5. Those limitations have been addressed above.

14. Regarding claims 6 and 9, the buffer controller controls all of the movement of data through the switch, so it is responsible for telling the output queues when to forward their data and for telling when the output queue should receive its data from the external memory (add signaling portion and a remove signaling portion). Also, the buffer controller can tell the output queue to access more data from the external memory by issuing a new port vector.

15. Regarding claim 17, it is inherent in Egbert et al. that the writing element would write the data cell into the output queue. Also, during operation, the output queue structure is acting most like a traditional queue, because it is from the portion that entries are taken, one by one. In a

traditional queue, the pointer will naturally increment in order to output the next piece of data. Step a3 has been mentioned previously.

16. Regarding claim 18, it is inherent in Egbert et al. that if the pointer is being incremented, then there must be some sort of add signal.

17. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Egbert et al.. Regarding claim 19, Egbert et al. does not expressly disclose incrementing a second entry counter. However, it would have been obvious to a person of ordinary skill in the art at the time of the invention to increment the second entry counter along with the first counter if another piece of data was to be transferred. One of ordinary skill in the art would have been motivated to do this because incrementing a separate counter could act as a confirmation for what the first counter value should be in case of an error in the system.

Allowable Subject Matter

18. Claim 11 is allowed. The closest prior art of record (Egbert et al.) discloses forwarding data before the data has been completely received, but Egbert et al. does not expressly disclose anything about providing a second signal to write information after a second predetermined threshold has been reached.

19. Claims 7, 10,and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Benson et al. (US 6,151,321), Burrows (US 5,303,302), and Higbee et al. (US 6,434,161) disclose systems when partial packets can be transferred to improve latency.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy Lee whose telephone number is (703)305-7349. The examiner can normally be reached on M-F, 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703)305-4744. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

TLL
July 7, 2003

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600